

Design of Tool for Exfoliation of Monocrystalline Micro-Scale Silicon Films

Ward, Martin

Department of Mechanical Engineering
University of Texas at Austin
204 E. Dean Keeton Street, Austin, TX 78712-1591
mjward@utexas.edu

Cullinan, Michael¹

Department of Mechanical Engineering
University of Texas at Austin
204 E. Dean Keeton Street, Austin, TX 78712-1591
michael.cullinan@austin.utexas.edu

ABSTRACT

This paper presents the development of a prototype exfoliation tool and process for the fabrication of thin-film, single crystal silicon, which is a key material for creating high-performance flexible electronics. The process described in this paper is compatible with traditional wafer-based, metal-oxide-semiconductor (CMOS) fabrication techniques which enables high performance devices fabricated using CMOS processes to be easily integrated into flexible electronic products like wearable or Internet of Things (IoT) devices. The exfoliation method presented in this paper uses an electroplated nickel tensile layer and tension-controlled handle layer to propagate a crack across a wafer while controlling film thickness and reducing the surface roughness of the exfoliated devices as compared with previously reported exfoliation methods. Using this exfoliation tool, thin-film silicon samples are produced with a typical average surface roughness of 75 nm and a thickness that can be set anywhere between 5 μm and 35 μm by changing the exfoliation parameters.

¹ Corresponding author

1. INTRODUCTION

The desire to integrate electronics into everyday products drives the need for flexible electronic devices in a broad range of applications, such as wearables [1,2] and IoT products [3]. As the sensing and computing needs for these types of applications become more complex, the flexible devices that get integrated into these products need to become more sophisticated [4], often requiring high-performance integrated circuits (ICs) for components like logic and radio communication. Flexible electronics are often manufactured using materials and fabrication methods that are inherently flexible, like oxide-based [5] or organic thin-film transistors fabricated on polymer substrates [6]. However, due to the instability of the polymer substrates and their incompatibility with high temperature processing, the electronics fabricated on polymer substrates are often of significantly lower quality than electronics fabricated using conventional CMOS processes. One alternative approach is to incorporate the rigid, high-performance, silicon-based ICs manufactured using traditional CMOS processes onto flexible substrates as small, discrete chips [7]. However, this approach suffers from difficulties with integrating silicon chips onto polymer substrates and reduces the overall flexibility of the electronic devices produced [3]. Thin-film, single-crystal silicon offers the potential to overcome both issues, since it is extremely flexible and CMOS compatible [3]. Therefore, thin-film, single-crystal silicon is an ideal material for the fabrication of large-area, high-performance flexible electronic devices.

There are several methods that have been used to fabricate thin-film, single crystal silicon, including chemical mechanical polishing (CMP) [8,9] and ion-beam

implantation, [10,11] but these approaches have disadvantages. For example, CMP requires that the entire backside of the wafer be ground down, which is a slow and expensive process, while ion-beam implantation does not allow for a device to be pre-fabricated on the bulk substrate before becoming a thin-film. Another promising technique for creating thin-film single crystal silicon that leverages existing CMOS infrastructure is exfoliation (also referred to as “kerfless-wafering” or “spalling”). In this process, the top layer of a silicon wafer is mechanically removed by brittle fracture, including any devices contained in that layer. The fracture is driven by a tensile layer placed on top of the bulk substrate that creates a stress concentration just below the surface. Once the stress intensity reaches the fracture toughness of the material, the crack will propagate. A similar phenomenon occurs as a mode of failure in other applications, where dissimilar coatings coupled with thermal stresses cause the substrate to fracture [12]. The stress intensity can be increased by raising the stress in the tensile layer or by applying an external load.

Several methods of exfoliation have been developed, each with a different method of creating the tensile stress and applying the final load. In 1986, Tanielian et al. [13] first mentioned exfoliation as means to produce thin-film single crystal silicon in a patent, but neither commercial results nor discussion in literature can be found. The patent describes a process that only uses thermal stresses in the tensile film to propagate the crack and does not implement any kind of control. A similar method was demonstrated by Dross et al. [14] using printed metal pastes which are thermally treated so that as the wafer cooled, the stress in the tensile film would increase until

sufficient energy was present to spontaneously generate and propagate the crack. R. Rao and L. Mathew [15–17] and D. Shahjerdi and S. Bedell [18–22] developed methods that added some control to the exfoliation process by introducing a wedge-type tool and a peeling handle layer, respectively. These processes will be discussed in further detail in the next section of this paper. The method of exfoliation presented in this paper combines features from those described above, but adds a critical element of control to the externally-applied loading by actively adjusting the tension in the peeling handle layer. This work focuses on the creation of a new exfoliation tool that repeatably creates high quality, uniform silicon films of a specified thickness.

2. BACKGROUND AND PREVIOUS METHODS

While exfoliation is a relatively new approach for obtaining thin-film single crystal silicon, several different methods and processes have recently been demonstrated. The methods vary in the way the tensile stress is applied to the silicon and the way the crack is propagated. This section will outline some of these previous approaches and their advantages and disadvantages.

2.1 Spontaneous Exfoliation

The first step in creating an exfoliation system is designing a tensile layer to apply concentrated stress to the silicon substrate. This stress is the primary source of energy for propagating the crack during exfoliation. In earlier methods, it was also the only source [14,23,24]. In these methods, a material with a different coefficient of thermal expansion from silicon was adhered to the silicon and the sample was heated to

induce stress. Eventually, a fracture would spontaneously initiate and abruptly release all the stored energy. The results of such methods have been reproduced and are shown in Figure 1.

As might be expected, when the large amount of energy stored in the system is suddenly released, multiple branching crack fronts are created. The resulting film is rough and non-uniform and may be damaged. The crystal anisotropy of the silicon also presents a challenge here because it creates preferential crack planes and directions. These effects can be seen in Figure 1 where the crack began spontaneously around the perimeter of the (100) wafer, but propagated along the preferred the $\langle 100 \rangle$ directions (top, bottom, left, and right edges in the image). These crack fronts also appear to collide, which creates a rougher surface finish at those intersection points. These results highlight the value in controlling the amount of energy the crack receives, as well as constraining the direction of propagation. Methods using directed thermal energy to control the crack propagation reduce the roughness [25,26], but further control and better surface finish are desired for high-performance IC applications.

2.2 Wedge Tool

An exfoliation method and process for creating cost-effective solar cells was developed at the University of Texas, Austin by AstroWatt Inc. and Applied Novel Devices Inc. [15–17]. This method uses a nickel tensile layer electroplated on top of an electron beam evaporated nickel seed layer with a titanium adhesion layer. The assembly is then heat-treated at a relatively low temperature which causes the microstructure of the electroplated nickel layer to change and produces a residual

tensile stress in the nickel after cooling. This method then uses a wedge tool that attempts to control the crack energy and crack propagation direction. The tool consists of a conveyor belt with a vacuum chuck attached to it and a thin wedge/blade. The wafer is placed on the chuck with the preferred orientation facing forward. In many situations, the wafer is too bowed due to the residual stress in the nickel layer to seal to the vacuum chuck, and it must be placed on a carrier wafer using a paraffin wax. The crack is then initiated manually by slightly lifting the edge of nickel. The conveyor belt then drives the wafer towards the wedge splitting mechanism, demonstrated in Figure 2.

In this mechanism, the wedge does not “cut” the silicon, since the tip of the wedge is not actually near the crack front. Instead, it propagates the crack by applying a prying load between the two surfaces, thus increasing the stress around the crack tip. This method improved the quality of the films. However, surface roughness and film thickness control are still problems due to friction and stick/slip conditions created by the wedge as well as dynamic motion in the exfoliated film behind the crack since this method only applies a displacement condition to the film and does not constrain the force at all.

2.3 Adhesive Tape Handle Layer

A similar process has been developed at IBM by D. Shahjerdi and S. Bedell [18–22] that uses an adhesive tape handle layer, as opposed to a wedge tool, to propagate a crack through the silicon wafer. This method also uses a nickel tensile layer, but DC magnetron sputtering, rather than electroplating, is used to deposit the layer.

Sputtering has the advantages of being able to produce a more uniform and consistent layer and has the ability to embed stress in the nickel layer during the deposition process without the need for a subsequent thermal process, but it is more costly and time-consuming compared to electroplating. In this method of exfoliation, no tool is used to perform the exfoliation. Instead, a handle layer of adhesive polyamide tape is placed on top of the nickel and simply peeled up by hand. Testing of this method showed improved smoothness compared to the wedge tool, but variations in the peeling motion could be observed as inconsistencies and ridges in the exfoliated surface. Maintaining a constant hand motion is difficult due to uncertainty in the required load necessary to propagate the crack. Ambiguity in the crack propagation direction is also present, because the load is being applied through an unconstrained compliant film across a relatively large distance which allows the crack to wander. The new tool incorporates the handle layer as an effective method of transferring energy to the crack tip.

3. PROTOTYPE TOOL DESIGN

The design of the exfoliation tool presented in this paper combines elements of each of the methods described in the previous section while introducing a new concept that can improve the overall quality of the exfoliated films. Mathew and Rao's solution controlled the direction of exfoliation and provided a controlled feed-rate, but the sliding wedge added noise to the crack front and roughness to the resulting films. Bedell and Shahrjerdi's solution partially controlled both the exfoliation rate and direction,

highlighting that applying loads through the handle layer was a viable option. The proposed controlled peeling concept presented in this paper combines the controlled feed-rate and handle film methods to repeatably add the minimum required energy to the crack while also steering it.

3.1 Controlled Peeling Concept

The controlled peeling concept uses two rollers to control the angle and tension in the handle film, as seen in Figure 3. The handle film is fixed to ground at one end and to the tensile layer at the other. Then the rollers are brought across the wafer using a linear actuator. This enables the tool to control the rate at which energy is added to the crack and constrains the film behind the crack. The tension in the handle layer and the height and orientation of the rollers can be adjusted to alter the loads applied to the tensile layer and the crack tip.

3.2 Peeling Model

To better understand the ideal load for the tool to apply, a 2D fracture mechanics model was created. Previous work in the field of thin-film interfacial fracture mechanics indicates that a stable crack path in the substrate is formed parallel to the wafer surface when the shear mode stress intensity, K_{II} , is equal to zero, and the opening mode stress intensity, K_I , is equal to a critical value, K_{Ic} [12] and that there is a characteristic crack depth for any given elastic system. The 2D fracture mechanics model is defined by the material properties of the Si and Ni, the crack length, the film thickness, and the film stress. Analytical solutions from [27,28] suggest that changing

the applied load can skew the mode mix ratio and, therefore, the characteristic crack depth. An analytical solution to the loading conditions created by the new tool was not feasible, so a parametric FEA model was created using ANSYS Fracture Tools that can be run iteratively to solve for the characteristic crack depth. A Kriging metamodel with increased accuracy around the solution was produced using adaptive sampling to vary the inputs. The metamodel allows the thickness of the silicon film to be predicted for a given set of inputs and helps inform the design of the tool by highlighting sensitivities. For example, analyzing the solutions revealed that the handle tension was a more effective input when the nickel stress and thickness were low. Details of the model and its results can be found in [29]. In Section 5, the results of the metamodel will be shown to help evaluate exfoliation results produced by the new controlled peeling tool.

3.3 Prototype Tool Architecture and Hardware

The prototype peeling tool was designed to be a cost-effective and modular method of quickly validating the controlled peeling concept. A layout of the tool in CAD is shown in Figure 4. The tool is constructed mainly from 1 inch (2.54 cm) aluminum t-slot extrusion based on an 18 x 18 inch (45.72 cm) optical breadboard. The two rollers from Figure 3 are attached to a rigid carriage, which slides on four linear bearings over two ground stainless steel shafts. The carriage's vertical distance above the wafer can be adjusted to set the roller height. The carriage is driven by a leadscrew and a machined Delrin nut which incorporates some radial compliance to compensate for the leadscrew's trueness. The leadscrew is driven by a high-torque gear motor mounted on isolating rubber mounts which is connected to the leadscrew by a belt and pulley system

to reduce the vibrations introduced into the system. The motor is driven by a basic open-loop pulse-width-modulation controller to set the exfoliation speed. The carriage was run at approximately 5-10 mm/min.

The handle film used for the exfoliation is clamped to the load cell and runs through the rollers as seen in Figures 5 and 6. The end of the handle film is attached to top of the wafer with a piece of adhesive tape. The tension in the handle film can be adjusted by placing weights on it. A rubber sheet can be added between the rollers and the wafer to help damp vibrations. The wafer is adhered to a rigid glass plate with a double-sided adhesive polyamide film, which is then secured in place with a vacuum chuck. The glass plate helps define the stress state and is necessary for wafers that are too bowed to be held by the vacuum chuck.

4. EXPERIMENTAL PROCEDURE

Sample preparation begins with 100 mm (100) silicon wafers which were cleaned and coated with a vapor deposited a 30 nm thick titanium adhesion layer and nickel seed layer. The wafers were then electroplated in a sulfamate bath to create the 10-35 μm nickel tensile layer. The tensile film properties are controlled primarily by the plating time and current density which ranged from 30-60 min and 15-25 mA/cm², respectively. Silicon exhibits its lowest fracture toughness in the {111} planes [30] and early tests exfoliating along this plane showed improved roughness. However, all testing was done with (100) wafers exfoliated in the <100> direction because they are cheaper and more common in device fabrication. After nickel plating, the perimeter of the wafer is trimmed using a laser cutter to remove the thick edges produced by the non-uniformity

of the electroplating process. The wafer is then heat-treated in an oven at 200-250 °C for 30 minutes. This treatment changes the microstructure of the nickel and the silicon substrate constrains the expansion of the nickel during this restructuring so that a residual tensile stress is induced in the nickel once it cools. At this point, the wafer is bowed from the residual nickel stress, so it is fixed to a rigid glass slide using double-sided polyimide tape to provide a flat surface which can be fixed to the exfoliation tool's vacuum chuck. The roller height can then be set using shims on top of the wafer. Once the wafer and rollers are in place, the handle layer is attached with adhesive tape to the front edge of the wafer and the tension is set and monitored with the load cell. To exfoliate the wafer, the carriage and rollers are moved across the wafer at a speed of approximately 8 mm/min.

5. RESULTS AND DISCUSSION

The new tool was tested on approximately 50 wafers to tune its parameters. Overall, the exfoliated films produced using this new tool show great surface finish and flexibility with a typical average surface roughness, S_a , of about 75 nm and a bend radius of less than 6 mm. The minimum bend radius has yet to be fully characterized and is highly dependent on the film thickness and substrate properties. An example wafer is shown in Figure 7a with a silicon film thickness of approximately 20 μm . Figure 7b shows a sample wrapped around a marker with a 6 mm radius. Figure 7c shows a thickness map of a silicon film, where the red lines are measured thickness data and the surface is a basic interpolation between these measurements to aid visualization of the topology of the exfoliated thin film. The thickness metrology was done using a combination of

dual KEYENCE LK-H207K laser displacement sensors and LEXT OLS4100 confocal microscope profile scans before nickel plating, after nickel plating, and after exfoliation. A modified Stoney's equation for silicon wafers [31] was used with the metrology data to calculate the tensile stress in the film. Details of the metrology process are described in [32]. The higher measured thickness around the edges of the sample is due to the electroplated nickel being thicker at the edges of the wafer due to non-uniformities in the nickel plating process. The nickel thickness and stress are the dominant control inputs for the crack depth, but crack depth can also be controlled by adjusting the tension in the handle film.

Reducing the roughness of the silicon film is desirable because it improves the conditions for any post processing and indicates a lower likelihood of damage in the silicon. Three samples were prepared using each of the exfoliation methods described in this paper (the wedge tool, tape peeled by hand, and the new controlled peeling tool) to create a roughness comparison between the different processes. Each sample was measured in 10 random locations using a Wyko NT 9100 optical profilometer and the compiled results are shown in Table 1.

Sample images from films produced using each method are shown in Figure 8. The wedge tool sample shows the highest average (S_a) and peak roughness (S_z) with low deviation. This indicates consistent large peaks in the surface which are also visible in the both interferometer image and photograph in Figure 8. The consistent peaks can be explained by a combination of the constant feed rate and the crack starting and stopping during the exfoliation process. As the wedge moves forward, the crack is pried

open until the stress intensity is high enough to cause the crack to advance, releasing the energy and restarting the process. The lack of a constraint on the foil behind the crack likely increases this effect. The interferometer image also appears to show increased roughness between the peaks compared to the other samples which may be due to friction and noise caused the silicon film slipping across the surface the wedge. The sample peeled by hand shows improved average roughness, but still has high peak roughness and high deviation, indicating infrequent but large peaks which are again visible in Figure 8. The start/stop effect of the wedge tool may also explain the inconsistent peaks in the hand-peeled sample, where imperfect hand motion causes the crack to stop and start, as well as energy being stored and released by the foil behind the crack. The controlled peeling tool solves these problems by maintaining a constant feed rate and exfoliation load while also maintaining a constant displacement of the foil behind the crack. As a result, it shows the lowest average and peak roughness and a low deviation, and both images show a smooth surface.

The controlled peeling tool demonstrates significant improvements in roughness, but thickness control is still required to consistently deliver usable devices. This control is achieved by using the metamodel described in Section 3.2 and [29] to first target a specific nickel thickness and nickel stress and then vary the tension in the handle layer to compensate for any errors in the nickel layer thickness/stress caused by the electroplating process. Figure 9 shows the profile of sample with a controlled step change in handle tension and compares the predicted silicon film thickness with the measured thickness on the left axis. The right axis gives the loading in the form of the

handle tension, nickel thickness, and nickel stress. The prediction uncertainty area is calculated by propagating metrology uncertainties through the metamodel and represents one standard deviation. The prediction appears to follow the measured silicon thickness trends over the nickel thickness and stress well, but slightly overestimates the effect of the handle tension. For the 30 N step change in handle tension shown, the metamodel predicted a 6 μm exfoliated film thickness while the actual change was closer 5 μm . This error may be caused by friction in the roller system that has not been accounted for in the metamodel. There is also non-uniformity in the measured crack depth profile that is uncorrelated to the nickel thickness, stress, and handle tension measurement profiles and may be caused by imperfections in the rollers and the tool's linear motion. However, this result demonstrates our tool's capability for controlling the silicon film thickness.

Figure 10 demonstrates the controlled peeling tool's ability to target and create very thin films showing a sample with an average measured thickness of 5.5 μm . The small peaks measured in the handle tension are due to instabilities in the film tensioning system of the prototype. The low film thickness is achieved by using the metamodel to tune the nickel thickness and nickel stress to target a thinner film and then increasing the handle tension to reach a minimum thickness. If the nickel thickness and nickel stress are used alone to control the film thickness, the variability in the electroplating process could send the crack irrecoverably towards the Si/Ni interface and cause a delamination of the nickel from the wafer. Therefore, using the handle tension as a fine control provides a more reliable method to consistently create very thin exfoliated films.

6. CONCLUSION

This paper introduced and successfully demonstrated a prototype tool design and process for creating thin-film silicon. The new tool shows improved roughness performance and better thickness control over previous methods of exfoliation. These improvements allow thinner silicon films to be created, which improves the flexibility of the finished thin-film devices. Together with the metamodel presented in [29], this controlled exfoliation tool creates the foundation for scalable fabrication of large-area single crystal silicon flexible devices. Options for future improvements include enhancing the crack steering control by actively controlling the tension on the handle film using a force feedback control system, improving the precision adjustment for height of the rollers using laser displacement feedback, and minimizing the noise and vibrations in the whole assembly by improving the mechanisms for linear motion and the quality of the rollers themselves. Variability in the nickel-plating process remains one of the largest obstacles in achieving full control of the exfoliation process. Future work involves creating controls on nickel plating as well as exploring other viable materials for the tensor layer. Possibilities include a spin-coated polymer or vapor-deposited layers. Different methods of applying and controlling the exfoliation force are also under investigation. For example, the stress state could be further modulated by manipulating the boundary condition at the base of the wafer. With this set of possible improvements, the controlled exfoliation process can become a cost-effective and viable method for manufacturing high-quality, flexible electronic devices.

ACKNOWLEDGMENT

The authors acknowledge and thank Miaomiao Yang for her experience, effort, insight, and support in accomplishing this work. The authors also thank Kirsten Cole Christopherson for her effort in completing these experiments and the authors would also like to thank Liam Conolly, Dipankar Behera, David Cayll, Cheng Zhao and all my lab mates for the informative discussions and technical expertise.

FUNDING

This work is based upon work supported primarily by the National Science Foundation under Cooperative Agreement No. EEC-1160494 and NNCI-1542159. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

NOMENCLATURE

| | |
|----------|----------------------------------|
| K_I | Mode I stress intensity |
| K_{II} | Mode II stress intensity |
| K_{Ic} | Mode I critical stress intensity |
| S_a | Average surface roughness |
| S_z | Peak surface roughness |

Accepted Manuscript Not Copyedited

REFERENCES

- [1] Ying, M., Bonifas, A. P., Lu, N., Su, Y., Li, R., Cheng, H., Ameen, A., Huang, Y., and Rogers, J. A., 2012, "Silicon Nanomembranes for Fingertip Electronics," *Nanotechnology*, **23**(34), p. 344004.
- [2] Kim, J., Lee, M., Shim, H. J., Ghaffari, R., Cho, H. R., Son, D., Jung, Y. H., Soh, M., Choi, C., Jung, S., Chu, K., Jeon, D., Lee, S.-T., Kim, J. H., Choi, S. H., Hyeon, T., and Kim, D.-H., 2014, "Stretchable Silicon Nanoribbon Electronics for Skin Prosthesis," *Nature Communications*, **5**, p. 5747.
- [3] Hussain, A. M., and Hussain, M. M., 2016, "CMOS-Technology-Enabled Flexible and Stretchable Electronics for Internet of Everything Applications," *Advanced Materials*, **28**(22), pp. 4219–4249.
- [4] Pang, C., Lee, C., and Suh, K.-Y., 2013, "Recent Advances in Flexible Sensors for Wearable and Implantable Devices," *J. Appl. Polym. Sci.*, **130**(3), pp. 1429–1441.
- [5] Fortunato, E., Barquinha, P., and Martins, R., 2012, "Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances," *Advanced Materials*, **24**(22), pp. 2945–2986.
- [6] Sirringhaus, H., 2014, "25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon," *Advanced Materials*, **26**(9), pp. 1319–1335.
- [7] Takei, K., Takahashi, T., Ho, J. C., Ko, H., Gillies, A. G., Leu, P. W., Fearing, R. S., and Javey, A., 2010, "Nanowire Active-Matrix Circuitry for Low-Voltage Macroscale Artificial Skin," *Nature Materials*, **9**(10), p. nmat2835.
- [8] Chaney, R., Hackler, D., Wilson, D., and Meek, B., 2013, "Flex Silicon-on-Polymer: Flexible (Pliable) ICs from Commercial Foundry Processes," *GOMAC*.
- [9] Hackler, D. D. R. H., and Chaney, R. L., 2015, "Semiconductor on Polymer Substrate."
- [10] Bruel, M., 1998, "The History, Physics, and Applications of the Smart-Cut® Process," *MRS Bulletin*, **23**(12), pp. 35–39.
- [11] Henley, F., Kang, S., Liu, Z., Tian, L., Wang, J., and Chow, Y.-L., 2009, "Beam-Induced Wafering Technology for Kerf-Free Thin PV Manufacturing," *Photovoltaic Specialists Conference (PVSC), 2009 34th IEEE*, IEEE, pp. 001718–001723.
- [12] Thouless, M. D., Evans, A. G., Ashby, M. F., and Hutchinson, J. W., 1987, "The Edge Cracking and Spalling of Brittle Plates," *Acta Metallurgica*, **35**(6), pp. 1333–1341.
- [13] Tanielian, M., Lajos, R. E., and Blackstone, S., 1986, "Method of Making Thin Free Standing Single Crystal Films."
- [14] Dross, F., Robbelein, J., Vandavelde, B., Van Kerschaver, E., Gordon, I., Beaucarne, G., and Poortmans, J., 2007, "Stress-Induced Large-Area Lift-off of Crystalline Si Films," *Applied Physics A*, **89**(1), pp. 149–152.
- [15] Rao, R. A., Mathew, L., Saha, S., Smith, S., Sarkar, D., Garcia, R., Stout, R., Gurmu, A., Onyegam, E., and Ahn, D., 2011, "A Novel Low Cost 25 μ m Thin Exfoliated Monocrystalline Si Solar Cell Technology," *Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE*, IEEE, pp. 001504–001507.
- [16] Mathew, L., and Jawarani, D., 2010, "Method of Forming an Electronic Device Using a Separation-Enhancing Species."

- [17] Zhai, Y., Mathew, L., Rao, R., Xu, D., and Banerjee, S. K., 2012, "High-Performance Flexible Thin-Film Transistors Exfoliated from Bulk Wafer," *Nano Letters*, **12**(11), pp. 5609–5615.
- [18] Bedell, S. W., Fogel, K., Lauro, P., Shahrjerdi, D., Ott, J. A., and Sadana, D., 2013, "Layer Transfer by Controlled Spalling," *Journal of Physics D: Applied Physics*, **46**(15), p. 152002.
- [19] Bedell, S. W., Shahrjerdi, D., Hekmatshoar, B., Fogel, K., Lauro, P. A., Ott, J. A., Sosa, N., and Sadana, D., 2012, "Kerf-Less Removal of Si, Ge, and III-V Layers by Controlled Spalling to Enable Low-Cost PV Technologies," *IEEE Journal of Photovoltaics*, **2**(2), pp. 141–147.
- [20] Bedell, S. W., Shahrjerdi, D., Fogel, K., Lauro, P., Hekmatshoar, B., Li, N., Ott, J., and Sadana, D. K., 2013, "(Invited) Cost-Effective Layer Transfer by Controlled Spalling Technology," *ECS Transactions*, **50**(7), pp. 315–323.
- [21] Shahrjerdi, D., and Bedell, S. W., 2013, "Extremely Flexible Nanoscale Ultrathin Body Silicon Integrated Circuits on Plastic," *Nano Letters*, **13**(1), pp. 315–320.
- [22] Shahrjerdi, D., Bedell, S. W., Khakifirooz, A., Fogel, K., Lauro, P., Cheng, K., Ott, J. A., Gaynes, M., and Sadana, D. K., 2012, "Advanced Flexible CMOS Integrated Circuits on Plastic Enabled by Controlled Spalling Technology," *Electron Devices Meeting (IEDM), 2012 IEEE International*, IEEE, pp. 5–1.
- [23] Schönfelder, S., Breitenstein, O., Rissland, S., De Donno, R., and Bagdahn, J., 2012, "Glue-Cleave: Kerfless Wafering for Silicon Wafers with Metal on Glueing and Removable Interface," *22nd Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes*.
- [24] Serra, J., Bellanger, P., Bouchard, P. O., and Bernacki, M., 2014, "Room Temperature Kerfless Silicon Thin Foils Obtained via a Stress Inducing Epoxy Layer: Room Temperature Kerfless Silicon Thin Foils Obtained via a Stress Inducing Epoxy Layer," *physica status solidi (c)*, **11**(11–12), pp. 1644–1647.
- [25] Hensen, J., Niepelt, R., Kajari-Schröder, S., and Brendel, R., 2015, "Directional Heating and Cooling for Controlled Spalling," *IEEE Journal of Photovoltaics*, **5**(1), pp. 195–201.
- [26] Niepelt, R., Hensen, J., Steckenreiter, V., Brendel, R., and Kajari-Schröder, S., 2015, "Kerfless Exfoliated Thin Crystalline Si Wafers with Al Metallization Layers for Solar Cells," *Journal of Materials Research*, **30**, pp. 3227–3240.
- [27] Suo, Z., and Hutchinson, J. W., 1989, "Steady-State Cracking in Brittle Substrates beneath Adherent Films," *International Journal of Solids and Structures*, **25**(11), pp. 1337–1353.
- [28] Drory, M. D., Thouless, M. D., and Evans, A. G., 1988, "On the Decohesion of Residually Stressed Thin Films," *Acta metallurgica*, **36**(8), pp. 2019–2028.
- [29] Ward, M., and Cullinan, M., 2019, "A Fracture Model for Exfoliation of Thin Silicon Flms," *Int J Fract.*
- [30] Tanaka, M., Higashida, K., Nakashima, H., Takagi, H., and Fujiwara, M., 2006, "Orientation Dependence of Fracture Toughness Measured by Indentation Methods and Its Relation to Surface Energy in Single Crystal Silicon," *International Journal of Fracture*, **139**(3–4), pp. 383–394.

- [31] Janssen, G. C. A. M., Abdalla, M. M., van Keulen, F., Pujada, B. R., and van Venrooy, B., 2009, "Celebrating the 100th Anniversary of the Stoney Equation for Film Stress: Developments from Polycrystalline Steel Strips to Single Crystal Silicon Wafers," *Thin Solid Films*, **517**(6), pp. 1858–1867.
- [32] Ward, M., 2018, "Wafer Scale Exfoliation of Monocrystalline Micro-Scale Silicon Films," Thesis.

Accepted Manuscript Not Copyedited

Table Caption List

Table 1 Average (S_a) and peak (S_z) surface roughness with one standard deviation for 10 measurements of a 4.2 mm^2 area for wafers exfoliated with the wedge-type tool, hand peeled with tape, and controlled peeling tool.

Accepted Manuscript Not Copyedited

Figure Captions List

- Fig. 1 Spontaneous exfoliation of a silicon thin film showing poor uniformity and surface finish.
- Fig. 2 Image of the wedge-type exfoliation tool and diagram of the wedge mechanism. The wedge pries the crack open but does not reach the crack tip.
- Fig. 3 Controlled peeling concept diagram. Rollers move the tensioned handle film over the wafer to exfoliate the film.
- Fig. 4 Prototype controlled peeling tool CAD rendering.
- Fig. 5 Prototype controlled peeling tool.
- Fig. 6 Close-up of exfoliation process and silicon thin-film.
- Fig. 7 (a) Sample test result at approximately 20 μm Si film thickness. (b) Bend radius demonstration. (c) Sample film thickness map.
- Fig. 8 Roughness comparison: (top) White light interferometer measurements of each method, (bottom) photographs of each sample. Note regular ridges on the wedge tool sample and irregular ridges on the hand peeled sample.
- Fig. 9 Example wafer measurement and prediction profile demonstrating crack depth control with step change.
- Fig. 10 Example wafer measurement and prediction profile targeting minimum thickness aided by metamodel prediction.

Table 1 Average (S_a) and peak (S_z) surface roughness with one standard deviation for 10 measurements of a 4.2 mm^2 area for wafers exfoliated with the wedge-type tool, hand peeled with tape, and controlled peeling tool.

| | Wedge Tool | Hand Peel | Roller Tool |
|--|-------------------|------------------|--------------------|
| S_a (nm) | 151 ± 21 | 107 ± 150 | 75.5 ± 21 |
| S_z (μm) | $3.46 \pm .5$ | 1.99 ± 1.7 | $1.15 \pm .8$ |

Accepted Manuscript Not Copyedited



Fig. 1 Spontaneous exfoliation of a silicon thin film showing poor uniformity and surface finish.

Accepted Manuscript Not Copyedited

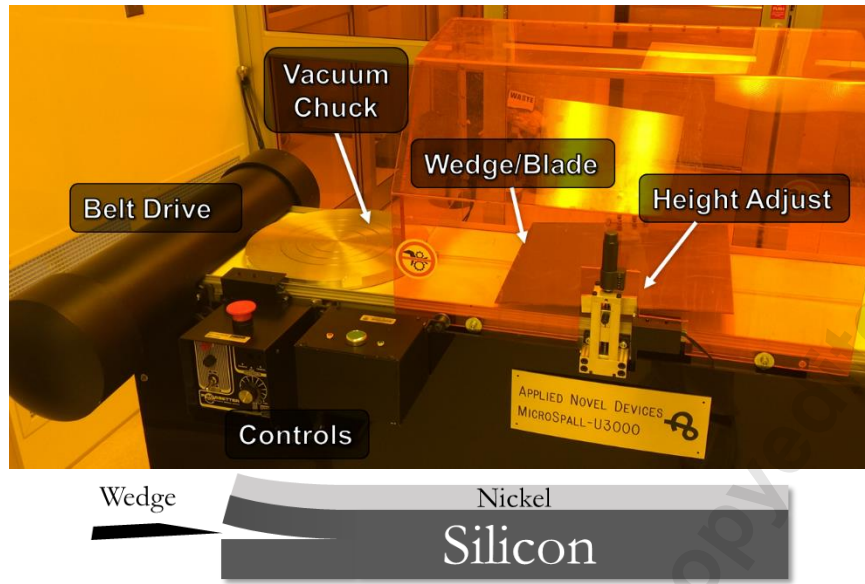


Fig. 2 Image of the wedge-type exfoliation tool and diagram of the wedge mechanism. The wedge pries the crack open but does not reach the crack tip.

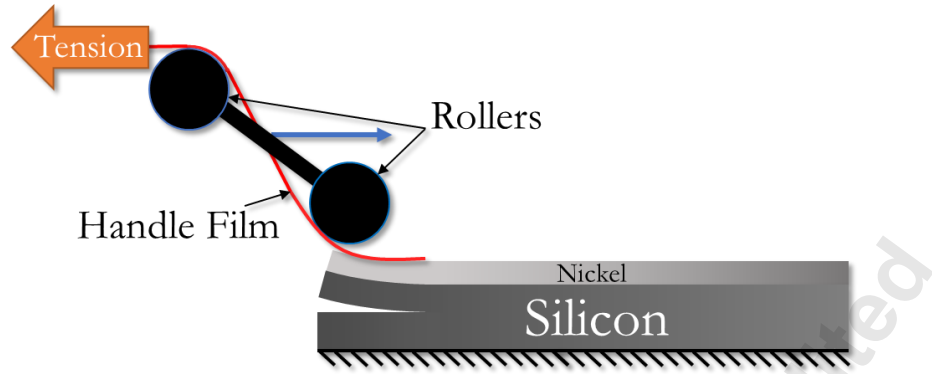


Fig. 3 Controlled peeling concept diagram. Rollers move the tensioned handle film over the wafer to exfoliate the film.

Accepted Manuscript Not Copyedited

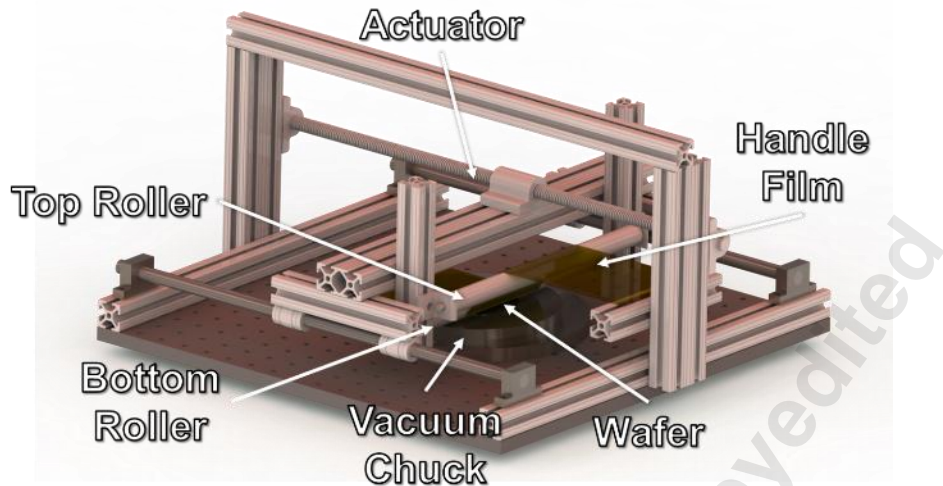


Fig. 4 Prototype controlled peeling tool CAD rendering.

Accepted Manuscript Not Copyedited

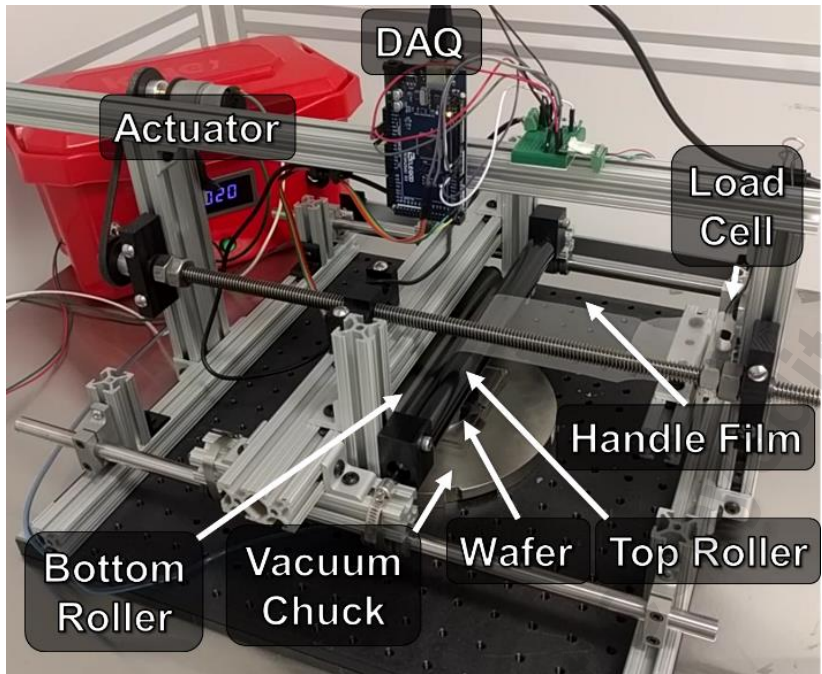


Fig. 5 Prototype controlled peeling tool.

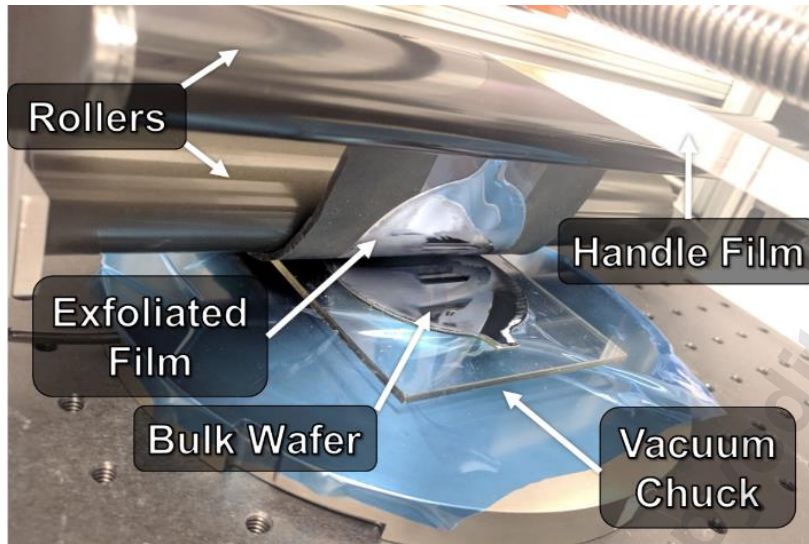


Fig. 6 Close-up of exfoliation process and silicon thin-film.

Accepted Manuscript Not Certified

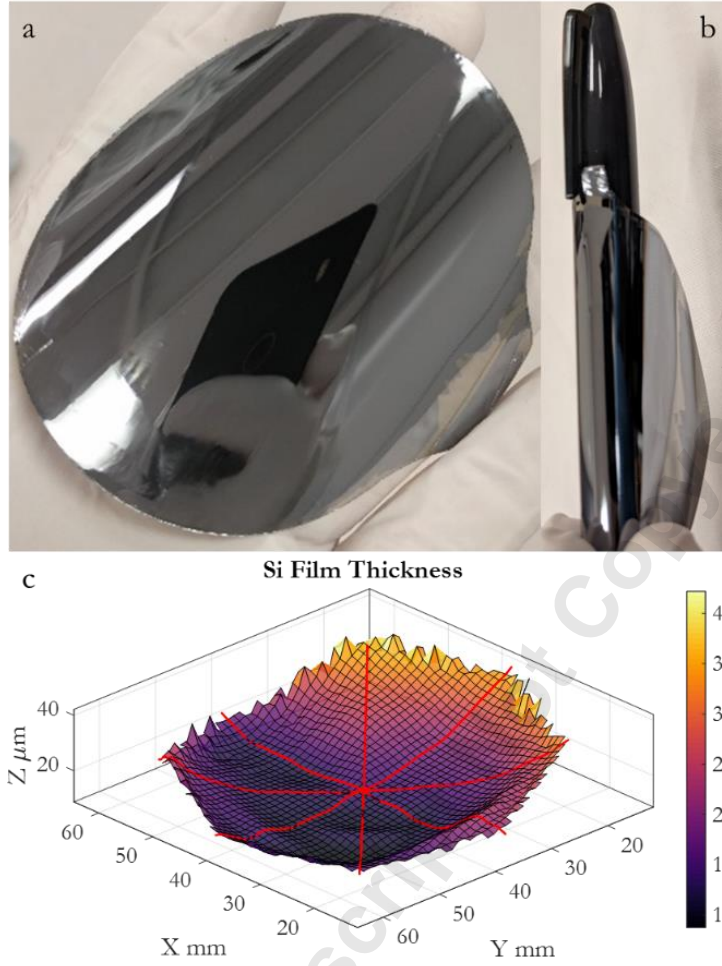


Fig. 7 (a) Sample test result at approximately $20\ \mu\text{m}$ Si film thickness. (b) Bend radius demonstration. (c) Sample film thickness map.

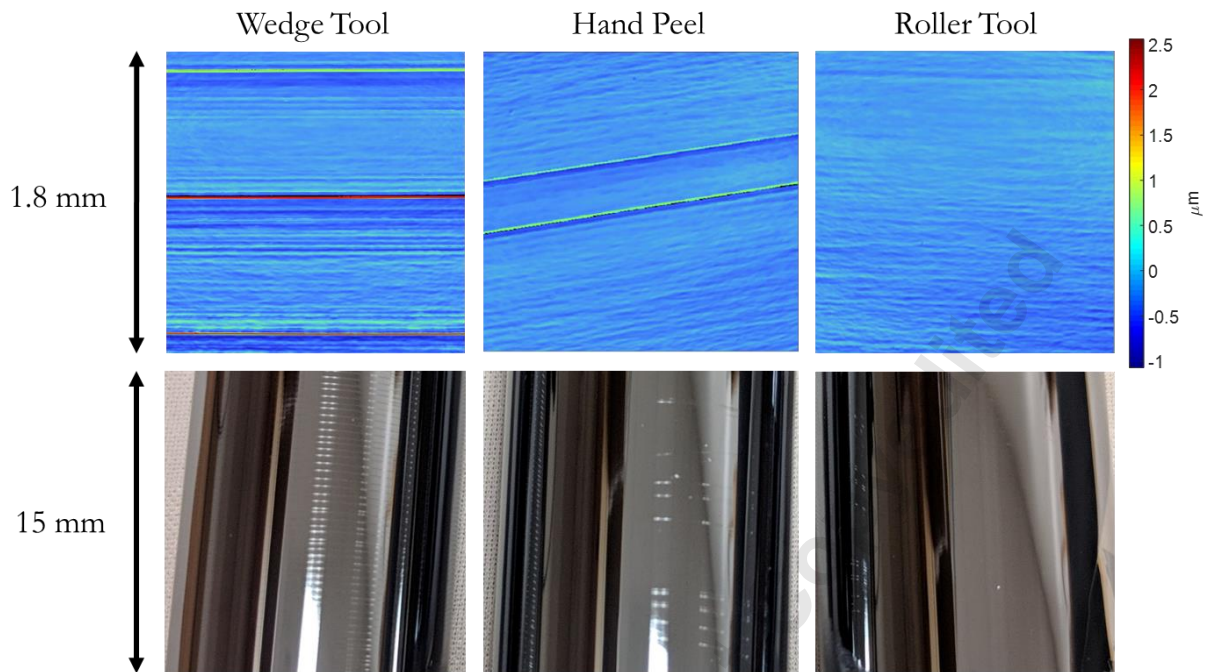


Fig. 8 Roughness comparison: (top) White light interferometer measurements of each method, (bottom) photographs of each sample. Note regular ridges on the wedge tool sample and irregular ridges on the hand peeled sample.

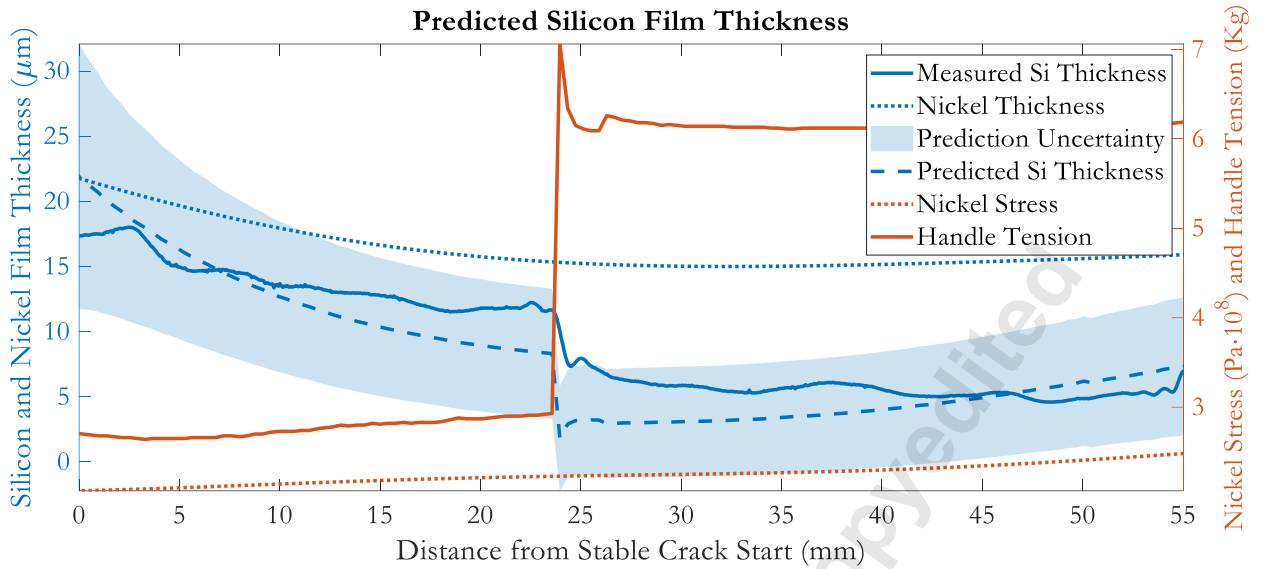


Fig. 9 Example wafer measurement and prediction profile demonstrating crack depth control with step change.

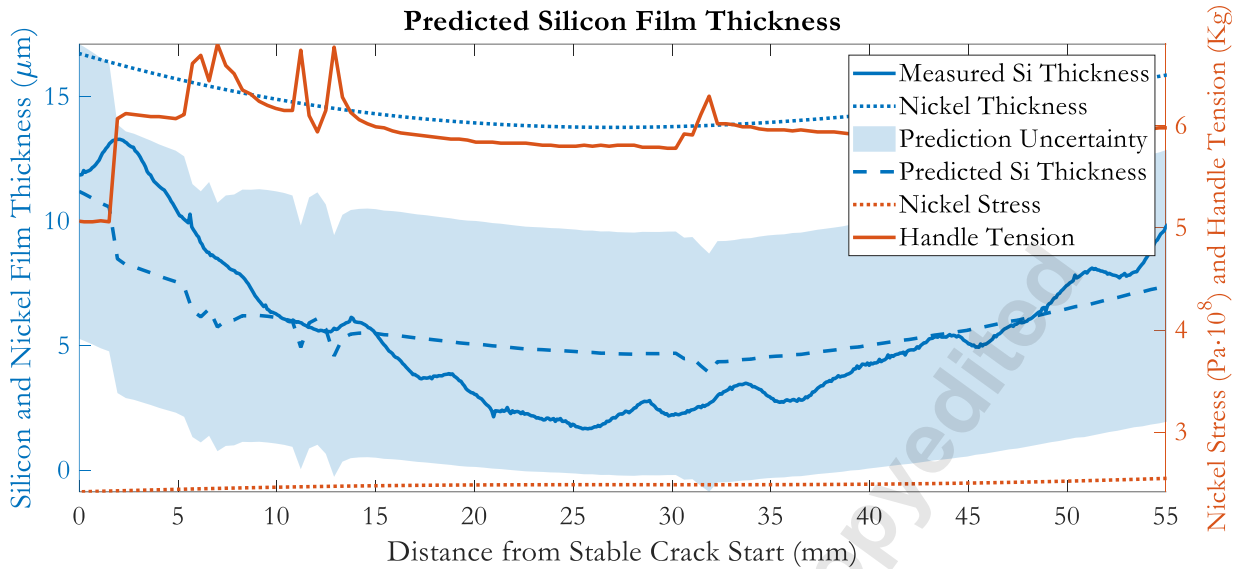


Fig. 10 Example wafer measurement and prediction profile targeting minimum thickness aided by metamodel prediction.